WHAT IS CLAIMED IS:

1. A transport interface for time division frames, in particular SDH frames, being transmitted between network nodes according to a specified transport protocol, said nodes comprising first circuit means for processing said time division frames according to said specified transport protocol, and second circuit means for exchanging second information streams with said first circuit means through said transport interface, wherein it comprises circuitry for structuring said second information streams as a data stream, sent in a co-directional way, and an address information.

2. A transport interface for time division frames, in particular SDH frames, according to claim 1, wherein the address information comprises an enable information of the exchange of the second information streams.

3. A transport interface for time division frames, in particular SDH frames, according to claim 2, wherein it provides for sending the data stream and address information with a reciprocal time delay.

4. A transport interface for time division frames, in particular SDH frames, according to claim 3, wherein it comprises a transmitter for sending a data stream, extracted from the time division frame, and first address information.

5. A transport interface for time division frames, in particular SDH frames, according to claim 3, wherein it comprises a receiver for receiving a data stream originated by the second circuit means and for sending second address information to said second circuit means.

6. A transport interface for time division frames, in particular SDH frames, according to claim 4, wherein said first address information comprises an enable information and one or more address information of the transmitted data stream.

7. A transport interface for time division frames, in particular SDH frames, according to claim 5, wherein said second address information comprises a transmission enable information for the second circuit means and one or more address information of the data stream requested from said second circuit means.

8. A transport interface for time division frames, in particular SDH frames, according to claim 6, wherein said first address information, in particular in the

instance of ATM data stream, comprises a synchronism signal, utilized by said second circuit means for marking the start of ATM cells and/or an alarm bit TSF for the second circuit means.

9. A transport interface for time division frames, in particular SDH frames, according to claim 7, wherein said second address information, in particular in the instance of an ATM data stream, comprises a synchronism signal for the first circuit means, for marking the correct bit of payload start, for a correct handling in the first circuit means of the information transported by the payload.

10. A transport interface for time division frames, in particular SDH frames, according to claim 1, wherein the first circuit means are implemented by a dedicated ASIC circuit, and the second circuit means are implemented by FPGA circuits.

11. A method for interfacing time division frames, in particular SDH frames, in a telecommunications networks, which provides for extraction and exchange of the data streams multiplexed in said time division frames between a time division frame processing circuit and devices for processing the data streams contained in said time division frames, wherein it provides for the step of allocating a data stream and an address information, for co-directional information exchange between the time division frame processing circuit and the processing devices.

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